# EMIF10-1K010F1

## EMI FILTER INCLUDING ESD PROTECTION

A.S.D.™

### MAIN APPLICATIONS

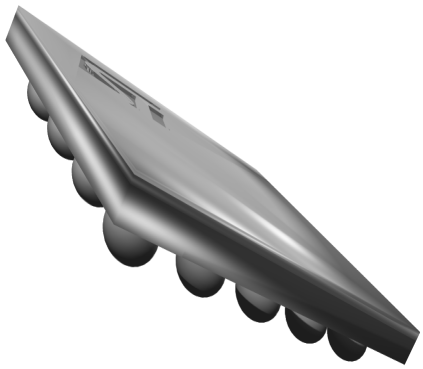
Where EMI filtering in ESD sensitive equipment is required:

- Computers and printers
- Communication systems
- Mobile phones
- MCU Boards

### DESCRIPTION

The EMIF10-1K010F1 is a highly integrated device designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 flip-chip packaging means the package size is equal to the die size. That's why EMIF10-1K010F1 is a very small device.

Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV.



**Flip Chip package**

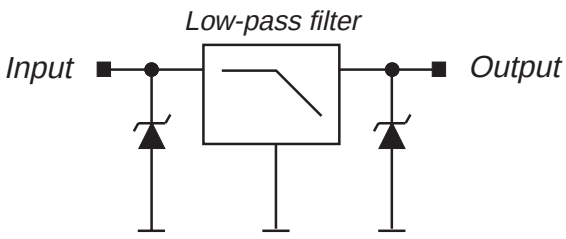
### BENEFITS

- EMI symetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 2.6 x 2.6 $mm^2$
- Very thin package: 0.65 mm
- High efficiency in ESD suppression on both input & output PINS (IEC61000-4-2 level 4).
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

### PIN CONFIGURATION (Ball Side)

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 1 | | I1 | I2 | O1 | O2 |
| 2 | I3 | I5 | I4 | O3 | O4 |
| 3 | GND | GND | I6 | O5 | O6 |
| 4 | GND | GND | I8 | O7 | O8 |
| 5 | I7 | I9 | I10 | O9 | O10 |

### BASIC CELL CONFIGURATION




*Ri/o = 1kΩ*

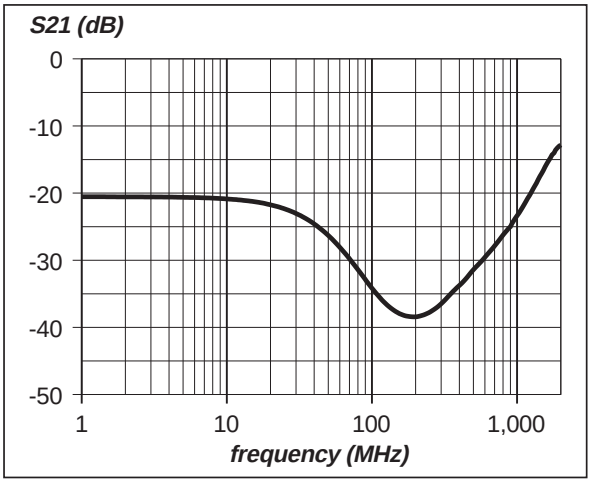
***Cinput = 100pF***

**TM** : ASD is a trademark of STMicroelectronics.

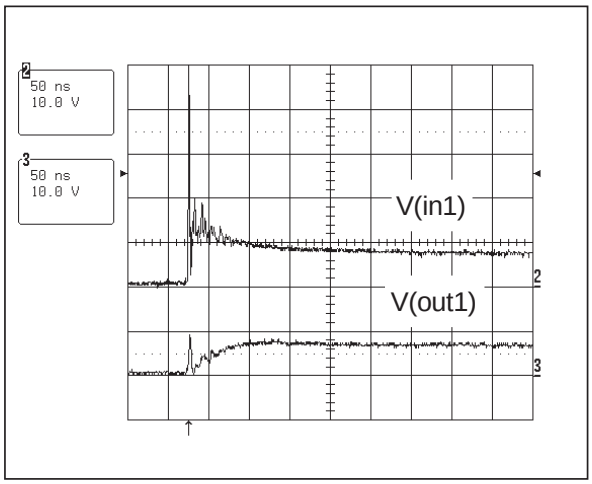
**COMPLIES WITH FOLLOWING STANDARD:**

IEC61000-4-2 level 4 15 KV (air discharge)
8 kV (contact discharge)
on input & output pins
MIL STD 883C - Method 3015-6 Class 3

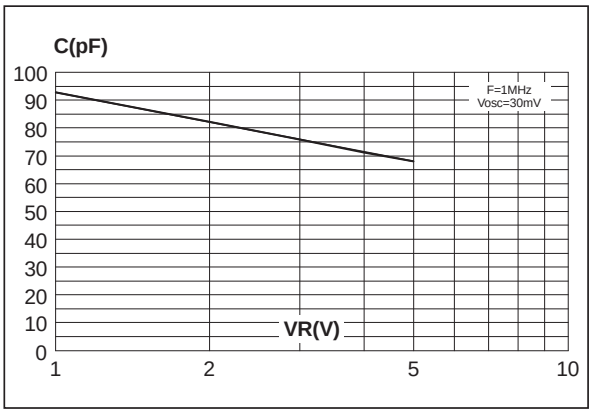
**Filtering Behavior**




**ESD response to IEC61000-4-2 (16kV Air Discharge)**




**Capacitance versus reverse applied voltage.**

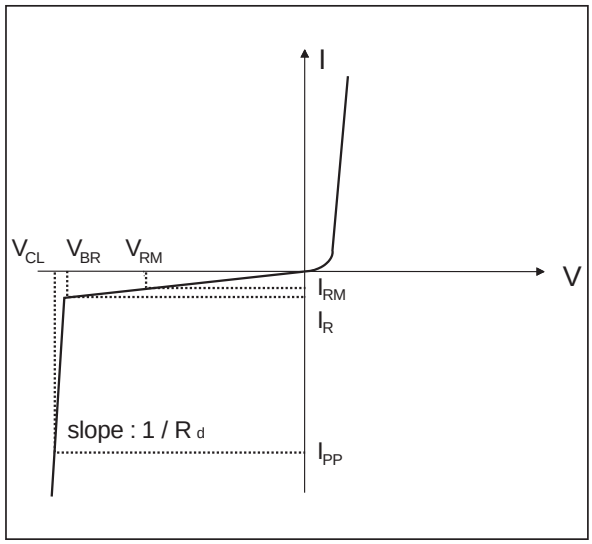


**ABSOLUTE MAXIMUM RATINGS** ($T_{amb}$ = 25 °C)

| Symbol | Parameter and test conditions | Value | Unit |
|---|---|---|---|
| $V_{PP}$ | ESD discharge IEC61000-4-2, air discharge<br>ESD discharge IEC61000-4-2, contact discharge<br>MIL STD 883C Method 3015-6 | 15<br>8<br>25 | kV |
| $T_j$ | Junction temperature | 125 | °C |
| $T_{op}$ | Operating temperature range | -40 to + 85 | °C |
| $T_{stg}$ | Storage temperature range | -55 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C)

| Symbol | Parameters |
|---|---|
| $V_{BR}$ | Breakdown voltage |
| $I_{RM}$ | Leakage current @ $V_{RM}$ |
| $V_{RM}$ | Stand-off voltage |
| $V_{CL}$ | Clamping voltage |
| $R_d$ | Dynamic impedance |
| $I_{PP}$ | Peak pulse current |
| $R_{I/O}$ | Series resistance between Input & Output |
| $C_{in}$ | Input capacitance per line |




| Symbol | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{BR}$ | $I_R$ = 1mA | 6 | 8 | 10 | V |
| $I_{RM}$ | $V_{RM}$ = 3V per line | | | 500 | nA |
| $R_d$ | $I_{PP}$ = 10A, $t_p$ = 2.5µs (see note 1) | | 1 | | Ω |
| $R_{I/O}$ | | 900 | 1000 | 1100 | Ω |
| Cline | At 0V bias | 80 | 100 | 120 | pF |

**Note 1**: To calculate the ESD residual voltage, please refer to the paragraph "ESD PROTECTION" on page 5.

## TECHNICAL INFORMATION

### FREQUENCY BEHAVIOR

The EMIF10-1K010F1 is firstly designed as an EMI / RFI filter. This low-pass filter is characterized by the following parameters:

- Cut-off frequency
- Insertion loss
- High frequency

Figure A1 gives these parameters, in particular the signal rejection at the GSM frequency:

- 25dB @ 900Mhz
- 14dB @ 1800Mhz

**Fig. A1:** Frequency response curve

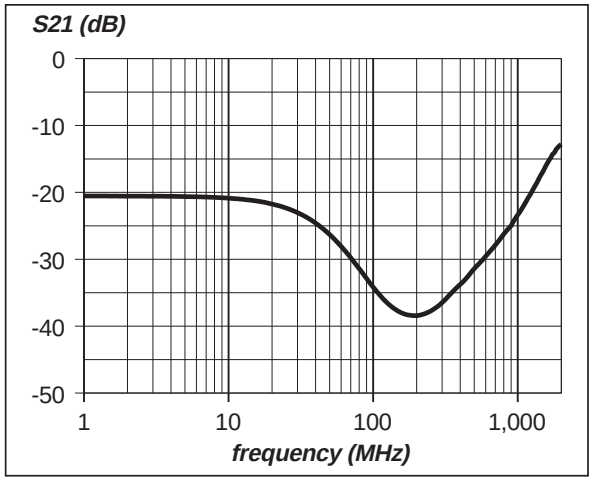
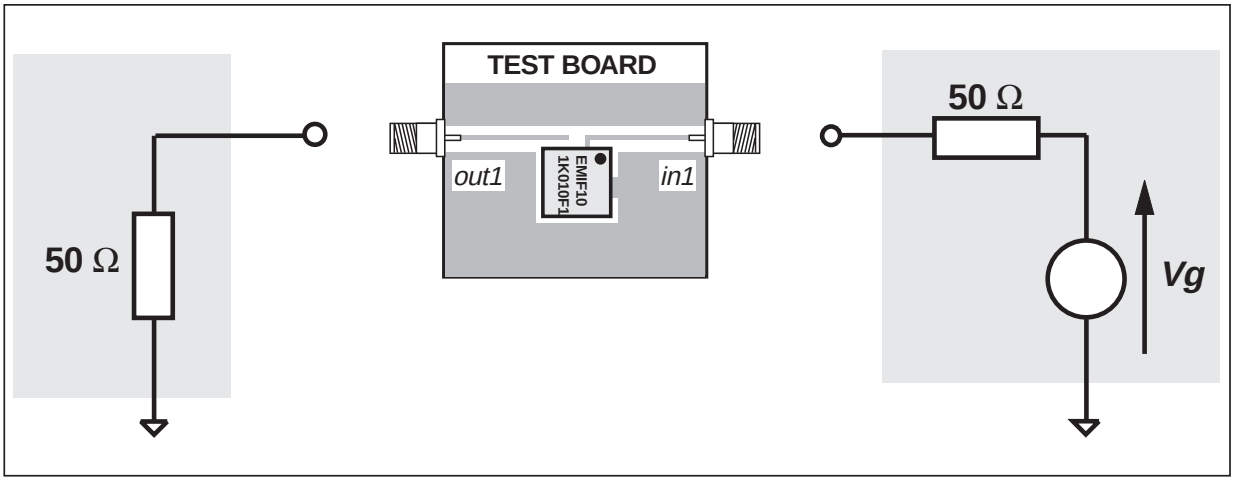



**Fig. A2:** Measurements conditions



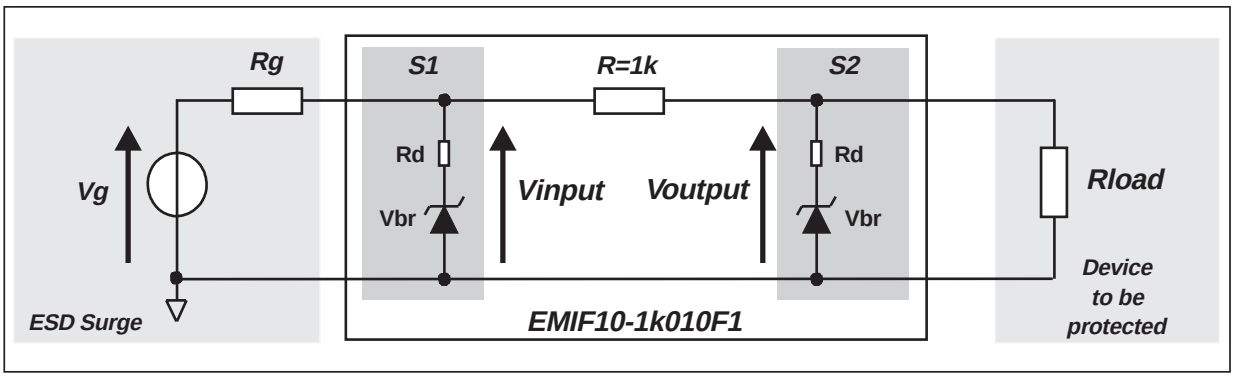
## ESD PROTECTION

In addition with the filtering the EMIF10-1K010F1 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at:

$$V_{cl} = V_{br} + R_d \cdot I_{pp}$$

This protection function is splitted in 2 stages. As shown in Figure A3, the ESD strikes are clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the output voltage very low at the Vout level.

**Fig. A3:** ESD clamping behavior




To have a good approximation of the remaining voltages at both Vin and Vout stages, we give the typical dynamic resistance value Rd. By taking into account these following hypothesis : R>>Rd, Rg>>Rd and Rload>>Rd, it gives these formulas:

$$Vinpout = \frac{R_g \cdot V_{br} + R_d \cdot V_g}{R_g}$$

$$Voutput = \frac{R \cdot V_{br} + R_d \cdot V_{in}}{R}$$

The results of the calculation done for an IEC 1000-4-2 Level 4 Contact Discharge surge (Vg=8kV, Rg=330Ω ) and Vbr=7V (typ.) give:

Vinput = 31.24V
Voutput = 7.03V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the Vin side. This parasitic effect is not present at the Vout side due the low current involved after the series resistance R.

## LATCH-UP PHENOMENA

The early ageing and destruction of IC's is often due to latch-up phenomena which mainly induced by dV/dt. Thanks to its RC structure, the EMIF10-1K010F1 provides a high immunity to latch-up by integration of fast edges. (Please refer to the response of the EMIF10-1K010F1 to a 3 ns edge on Fig. A9)

The measurements done here after show very clearly (Fig. A5a & A5b) the high efficiency of the ESD protection :

- almost no influence of the parasitic inductances on Vout stage
- Vout clamping voltage very close to Vbr for positive surge and close to ground for negative one

**Fig. A4:** Measurement conditions

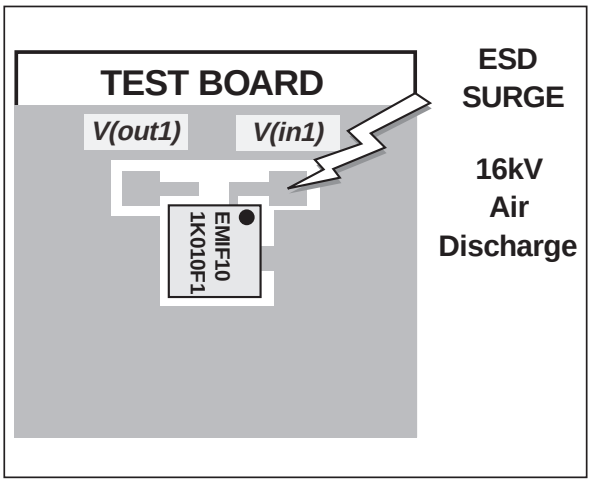
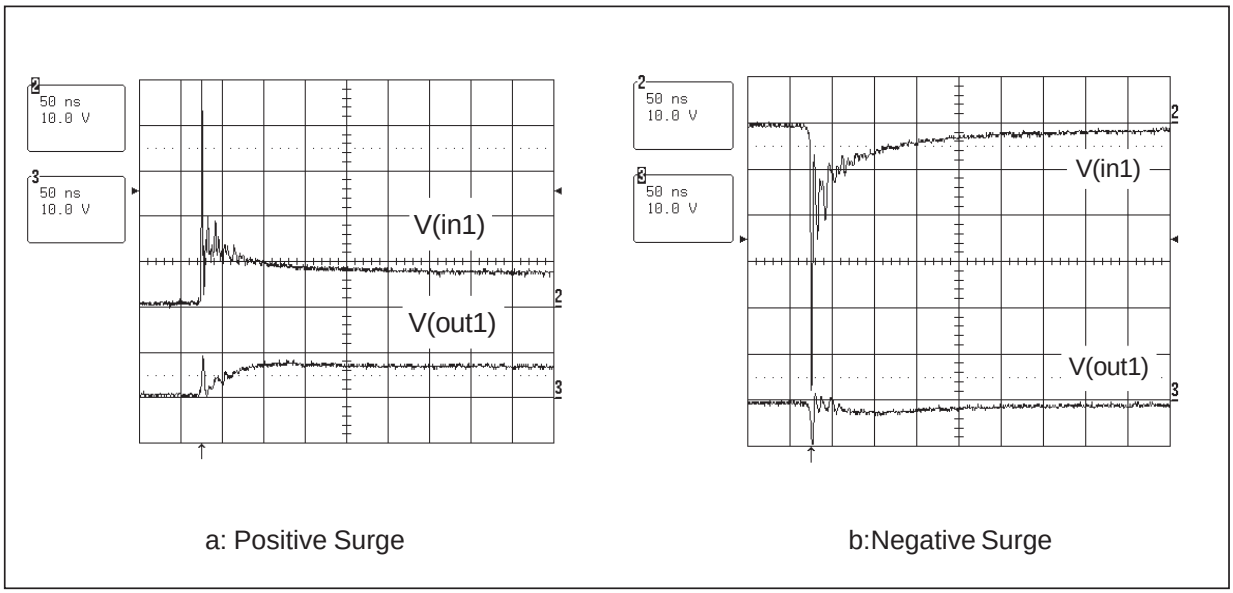



**Fig.A5:** Remaining voltage at both stages S1 (Vin1) and S2 (Vout1) during ESD surge



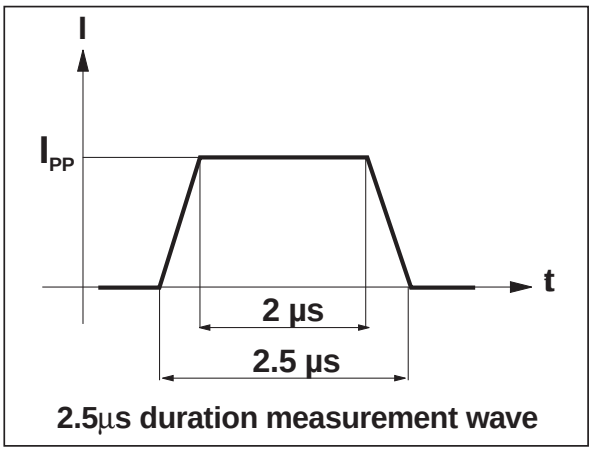

a: Positive Surge

b:Negative Surge

Please note that the EMIF10-1K010F1 is not only acting for positive ESD surges but also for negative ones. For negatives surges, it clamps close to ground voltage as shown in Fig. A5b.

**Note**: Dynamic resistance measurement

**Fig. A6:** Rd measurement current wave



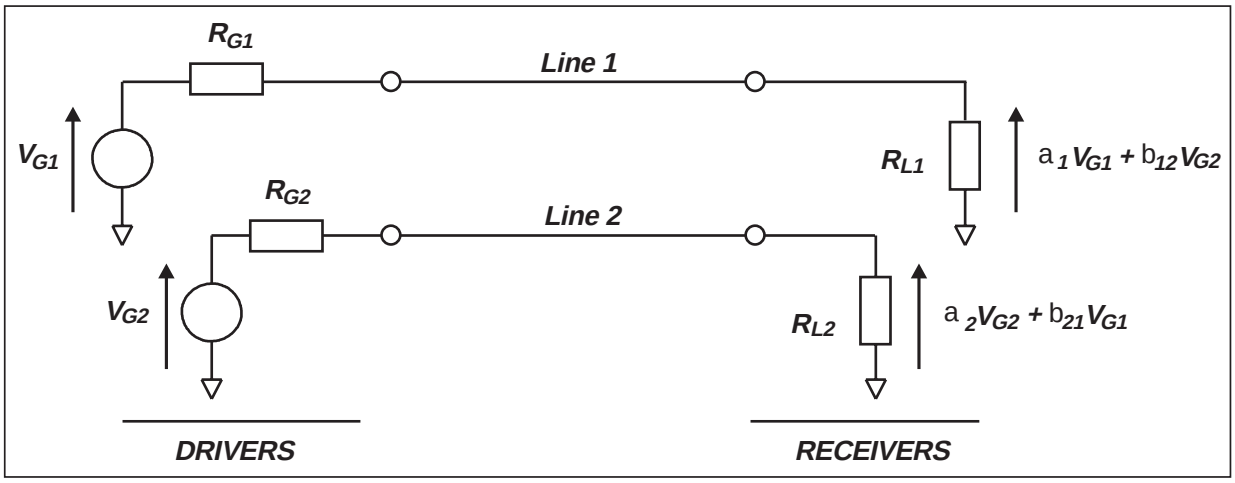

**2.5µs duration measurement wave**

As the value of the dynamic resistance remains stable for a surge duration lower than 20µs, the 2.5µs rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd

## CROSSTALK BEHAVIOR

### 1 - Crosstalk phenomena

**Fig. A7:** Crosstalk phenomena




The crosstalk phenomena are due to the coupling between 2 lines. The coupling factor ($\beta_{12}$ or $\beta_{21}$ ) increases when the gap across lines decreases, particularly in silicon dice.
In the example above the expected signal on load $R_{L2}$ is $\alpha_2 V_{G2}$, in fact the actual voltage at this point has got an extra value $\beta_{21}V_{G1}$. This part of the $V_{G1}$ signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2.
This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kW). The following chapters give the value of both digital and analog crosstalk.

## 2 - Digital Crosstalk

**Fig. A8:** Digital crosstalk measurement

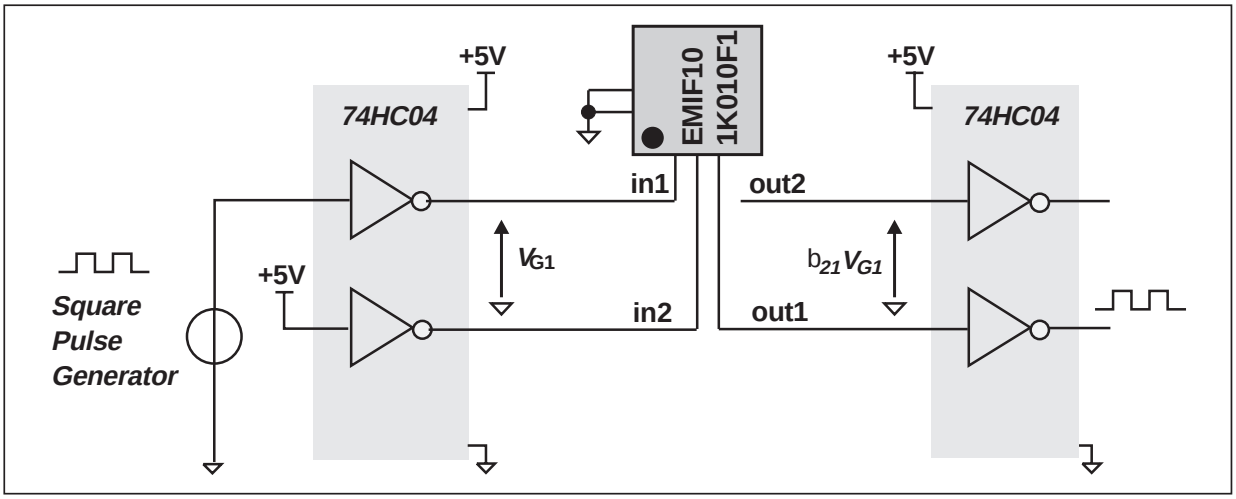
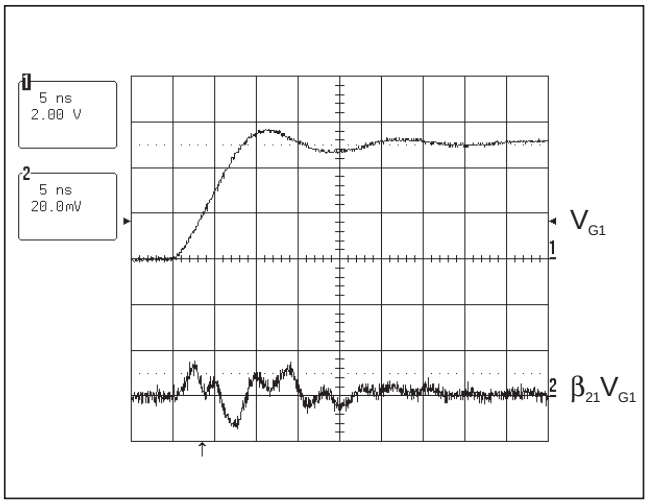



Figure A8 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Figure A9 shows that in such a condition signal from 0 to 5V and rise time of few ns, the impact on the disturbed line is less than 40mV peak to peak. No data disturbance was noted on the concerned line.

The measurements performed with falling edges gives an impact within the same range.

**Fig. A9:** Digital crosstalk results



### 3 - Analog Crosstalk

**Fig. A10:** Analog crosstalk measurement

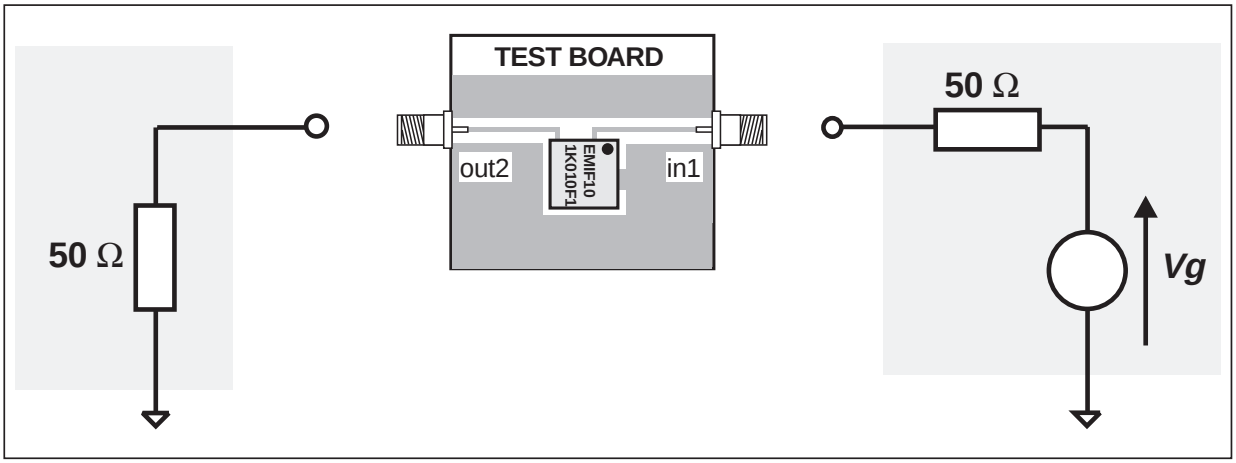



**Fig. A11:** Typical analog crosstalk results

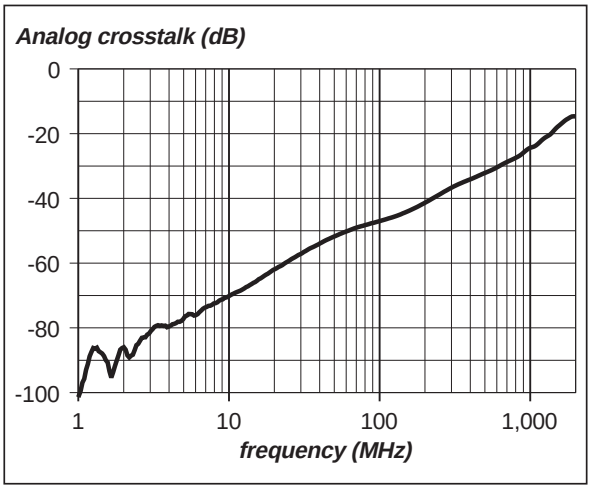
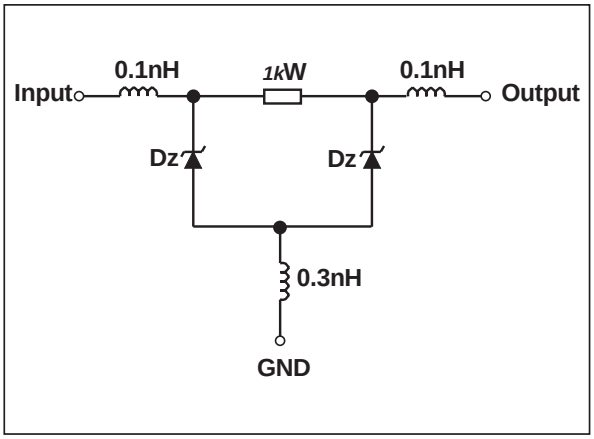



Figure A10 gives the measurement circuit for the analog application. In Figure A11, the curve shows the effect of cell I1/O1 on cell I2/O2. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -47 dB.

## 4 - Spice model

**Fig. A12:** Spice model of one EMIF01 cell

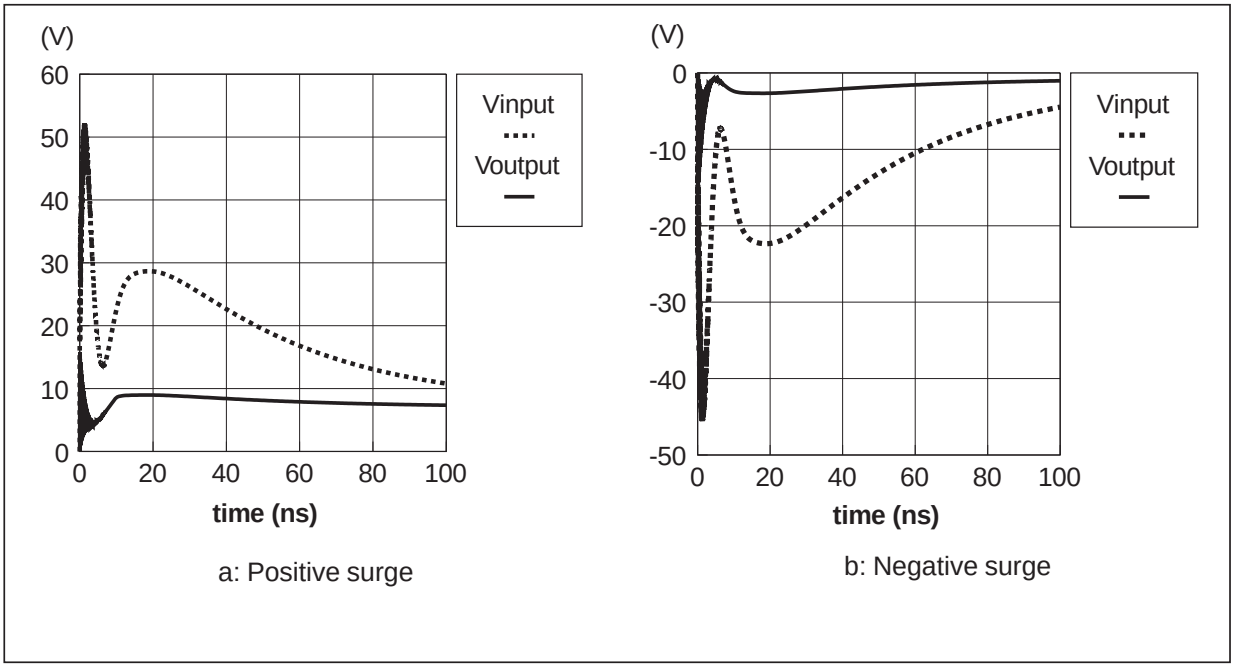



**Note:** this model is available for an ambient temperature of 27°C.

**Fig. A13:** Diodes Spice parameters

| | DZ |
|---|---|
| BV | 7 |
| Cjo | 50p |
| IBV | 1m |
| IKF | 1000 |
| IS | 10E-15 |
| ISR | 100p |
| N | 1 |
| M | 0.3333 |
| RS | 1 |
| VJ | 0.6 |
| TT | 100n |

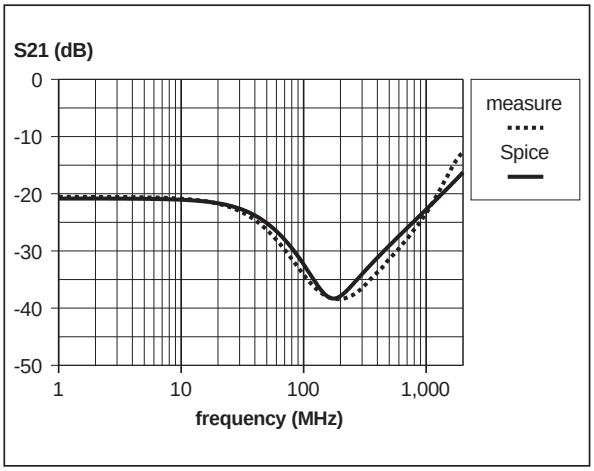
**Fig. A14:** Spice simulation: IEC 1000-4-2 Level 4 Contact Discharge response




a: Positive surge

b: Negative surge

**Fig. A15:** Comparison between PSpice simulation and measured frequency response.




## 5 - Aplac model

**Fig. A16:** Aplac model of one EMIF10 cell.

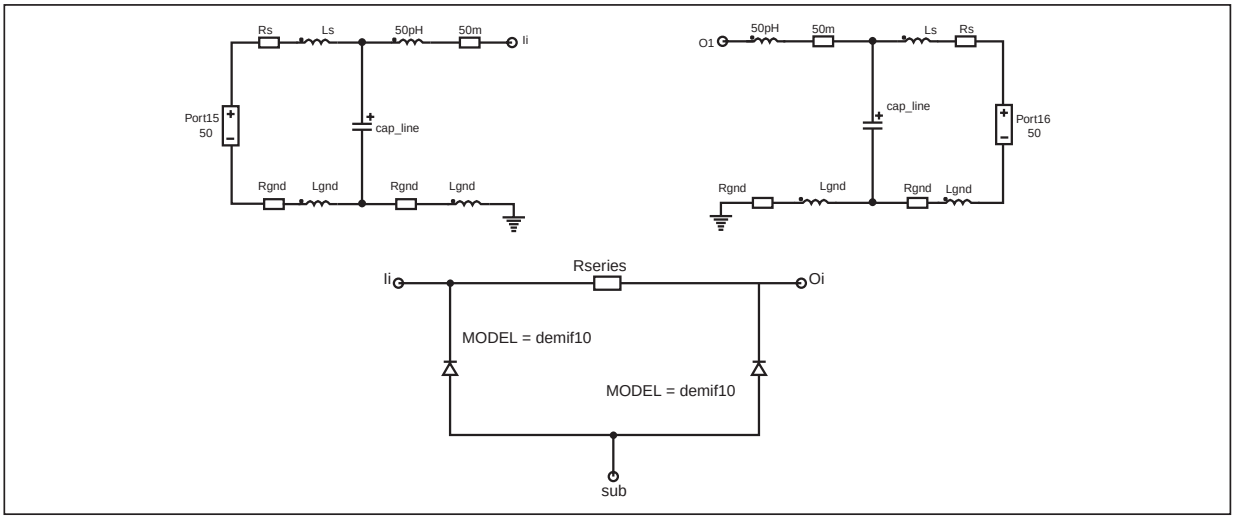



**Fig. A17:** Aplac model of bump connections.

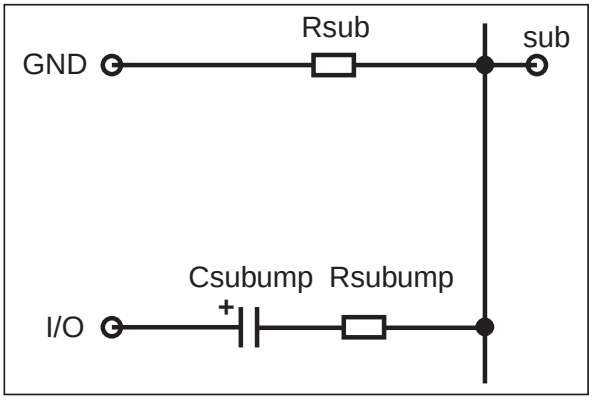



**Fig. A18:** Aplac model of ground connections.

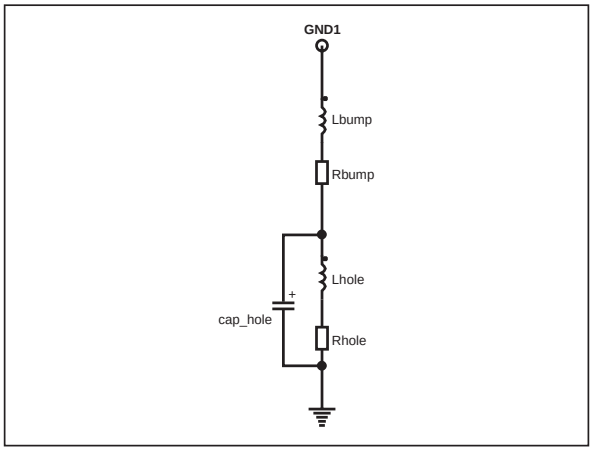
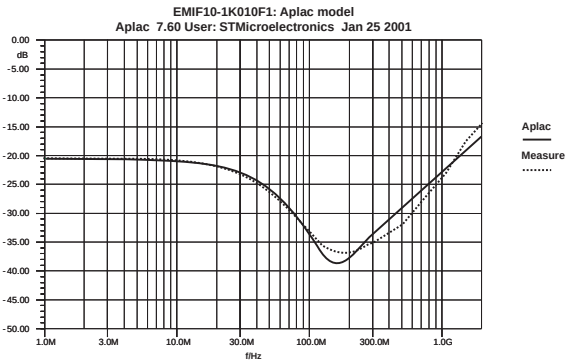


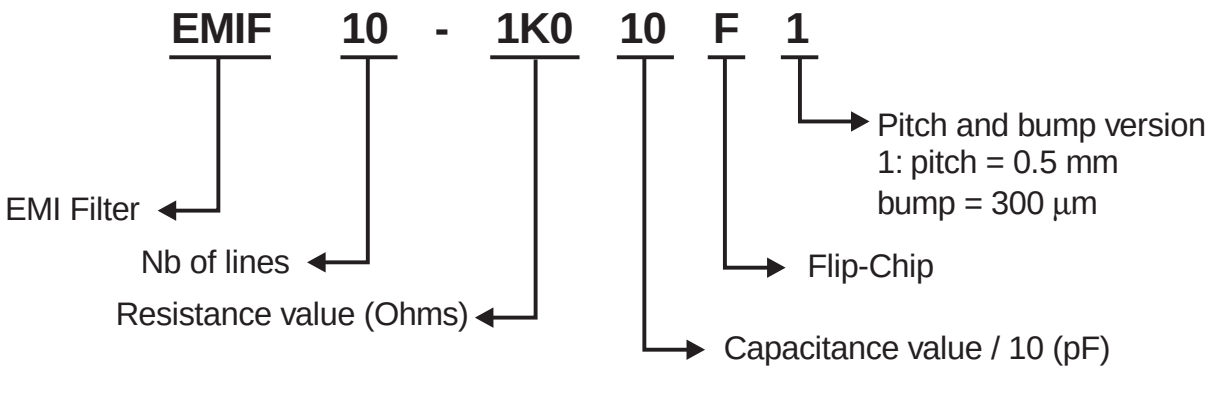
**Fig. A19:** Aplac model parameters.

```
aplacvar Cz 57pF                    Demif10 diodes model
aplacvar Rseries 960                BV=7
aplacvar cap_line 0.8pF             IBV=1m
aplacvar Ls 0.6nH                   CJO=Cz
aplacvar Rbump 50m                  M=0.3333
aplacvar Lbump 50pH                 RS=1
aplacvar Rs 0.15                    VJ=0.6
aplacvar Csubump 1.5pF              TT=100n
aplacvar Rsubump 0.15
aplacvar Rsub 0.1
aplacvar lhole 1.2nH opt
aplacvar Rhole 0.15
aplacvar cap_hole 0.15pF
aplacvar Rgnd 0.25
aplacvar lgnd 0.4nH
```

**Fig. A20:** Comparison between Aplac simulation and measured frequency response.



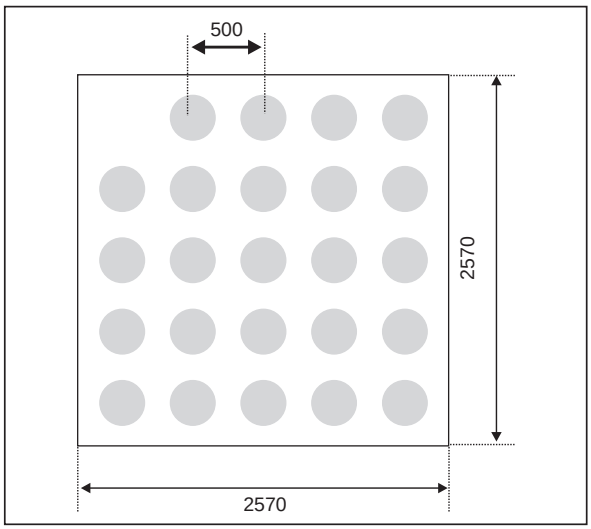

## ORDERING CODE

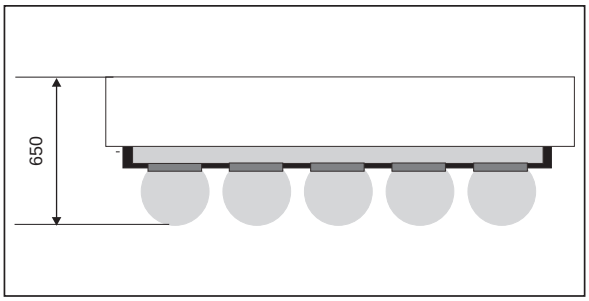


## PACKAGE MECHANICAL DATA

All dimensions in µm

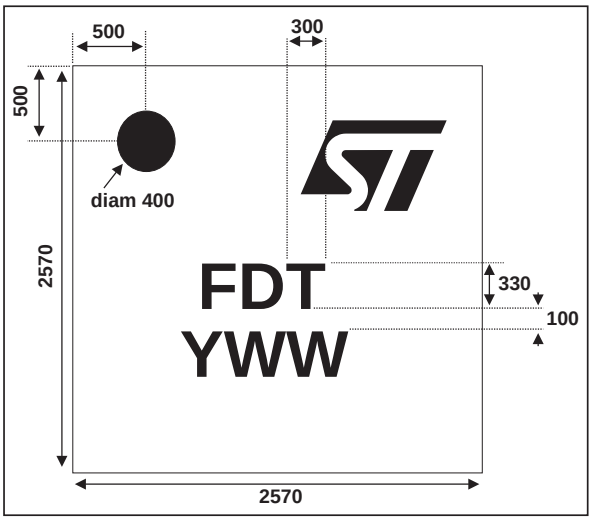
### DIE SIZE




- Die size: (2570 ± 50) x (2570 ± 50)
- Die height (including bumps): 650 ± 65
- Bump diameter: 315 ± 50
- Pitch: 500 ± 50
- Weight: 9.2mg

### MARKING




- Bottom side (balls view): Pin A1 missing for die orientation
- Top side (balls underneath): see the marking on the left.

- YWW: Date code

### PACKING:

EMIF10-1K010F1 is delivered in Tape & Reel (7 inches reel); one Tape & Reel contains 5000 dice.

**Note:** More packing information are available in the application note AN1235: "Filp-Chip package description and recommandations for use"